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DESIGN OF LOW-POWER FULL ADDER IN 0.18 µm CMOS TECHNOLOGY

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ABSTRACT

With the increase in device integration level and the growth in complexity of Integrated circuits, small delay and low power dissipation become important parameters as these increases performance and portability. Battery storage is limited, to extend battery life; low power operation is the primary requirement in integrated circuits. Furthermore, high speed and multiple parallel applications need high computing power, placing greater demands on energy storage elements within the system. Large power dissipation in high performance digital systems requires large size heat sinks. These off chip component makes chip bulky and require large space. Secondly, extra heat in integrated circuit degrades the system performance. The full adder (FA) is a very important and basic building block in Arithmetic and Logic unit (ALU) of digital processor. The most widely accepted metrics to measure the quality of a digital circuit or to compare various circuit styles is power delay product. Further, Portability imposes a strict limitation on power dissipation while needs more computational speeds. The reduced power consumption and the improved speed require optimizations at all levels of the design procedure.

CMOS technology has low power dissipation. Many researchers have developed various logic styles to implement Full Adder such as conventional static CMOS, dynamic CMOS, transmission gates, NORA[38] which has various advantages and limitation. Conventional Static CMOS has been used in much processor design. Static Pass Transistor circuit can also be used for Low Power applications. Dynamic circuit is also useful in Low Power high speed systems with careful clocking. Reversible logic is also noticeable recently for reducing the power dissipation. Quantum arithmetic component design requires reversible logic circuits. Reversible logic circuits has several applications such as in low power digital design, nanotechnology , DNA and quantum computing.

In the proposed work, the limitation associated with the above mentioned design style are studied and the transistor count reduction is done to reduce the power dissipation. The newly proposed structures will be simulated using SYMICA simulator software and 0.18 µm CMOS technology is selected for simulation. The proposed design will definitely reduce the power dissipation at-least 20%.

KEYWORDS: Power reduction,CMOS, GDI, PTL, symica simulator.

INTRODUCTION

In the past years, the VLSI designers targeted the performance and miniaturization mainly. High power consumption is an alarming issue with the substantial growth in portable electronics devices. There are problems with heat removal and cooling of the device as the power dissipation per unit area increases with scaling. The portable battery-operated electronic devices were initially known by low computational requirement. But, recently there is a need of high computational performance by the applications. It is therefore important to extend the battery life. With these reasons power dissipation is very important issue for circuit designers[44].

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Static power dissipation from standby leakage currents is an critical parameter of total power dissipation. Electronic devices have different types of component and some of them may remain inoperative during a specific operation. Large percentage of total power dissipation in the system is due to the static power dissipation in these inoperative components. The performance of MOS devices is remarkable enhanced due to the continued scaling of MOS devices,. This infact increased the power dissipation due to leakage currents. Now, this leakage component becomes an important parameter for power efficient system. Also, there is continuous evolution of low power and low voltage CMOS VLSI circuits day-by-day.

Full Adder

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. Beside three inputs, it has two outputs two of the input variables denoted by A and B, represent the two significant bits to be added. The third input, C_{in}, represents the carry from the lower significant position. Two outputs are necessary because the arithmetic sum of three bits ranges in value from 0 to 3 and binary 2 and 3 need two digits for their representation again, the two outputs are designated by the symbol 'S' for SUM and 'C_{out}' for carry output. The simplified sum-of-product functions for the two outputs are

$$S=\bar{A}.\bar{B}.C_{in}+\bar{A}.B.\overline{C_{in}}+A.\bar{B}.\overline{C_{in}}+A.B.C \quad (1)$$

$$C_{out}=A.B+B.C_{in}+C_{in}.A \quad (2)$$

MATERIALS AND METHODS

PREVIOUS WORK

A. 28T CMOS FULL ADDER:

This adder is based on CMOS structure (pull-up and pull-down network).

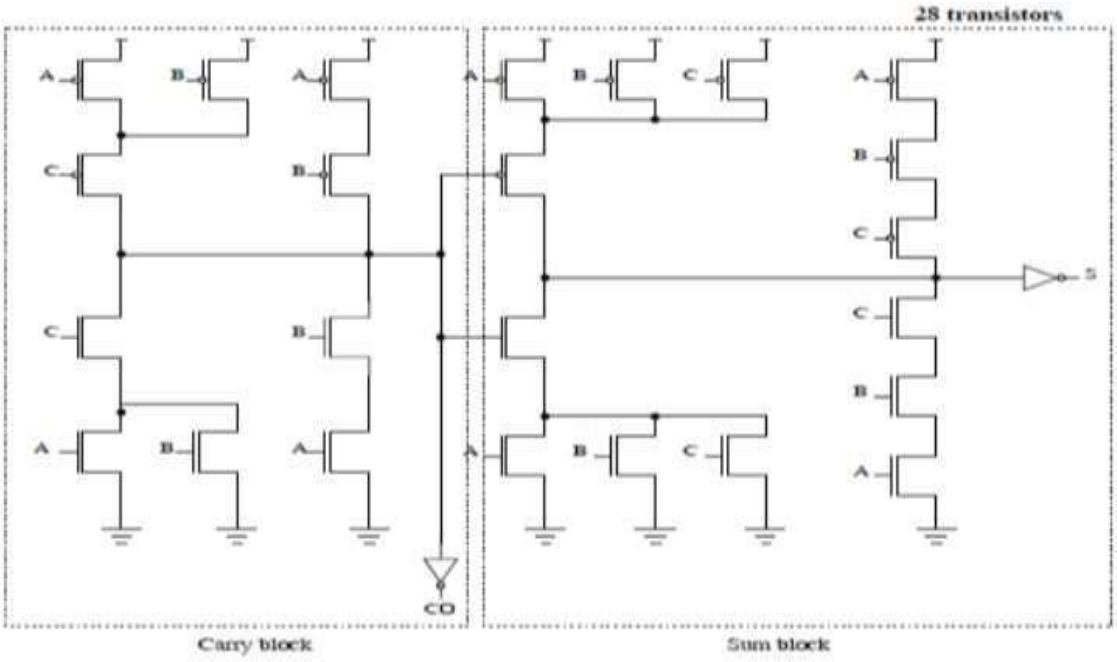

Fig. 1.Conventional 28-T CMOS full adder[19].

C_{out} is generated first then the sum is derived. One of the most significant advantages is the higher noise margins and in turn reliable low voltage operation. The larger number of transistors results in increased input loads, higher power consumption and more silicon area[19].

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B. 20 T TRANSMISSION GATE FULL ADDER:

It produces buffered outputs with proper polarity with the disadvantage of high power consumption.

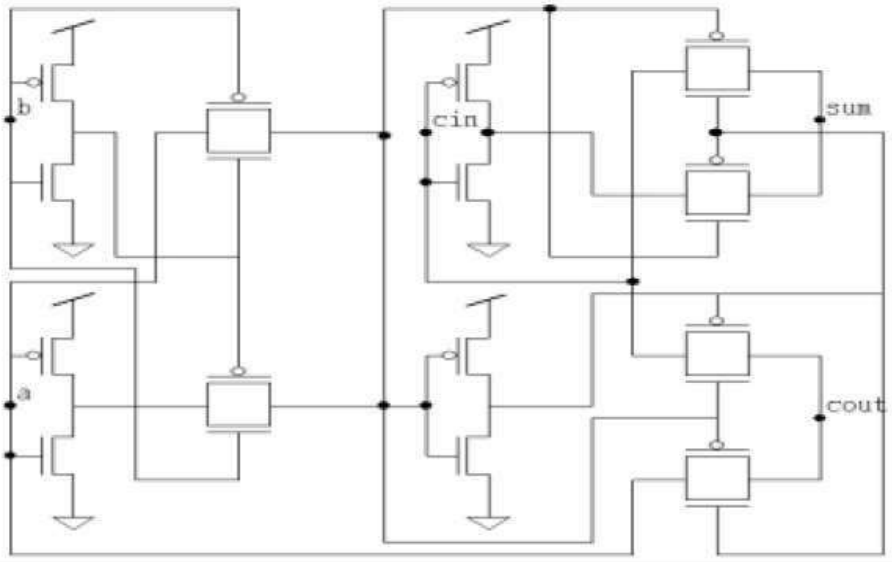

Fig. 2.-T transmission Gate Full Adder[19][28].

In this design 2 inverters with two transmission gates are used which act as 8-T XOR and 8-T XNOR module . To generate Sum; C_{in} and C_{in}' are multiplexed controlled either by (a ⊕ b) or (a ⊕ b)'.Similarly the C_{out} is the multiplexed output of A and C_{in} controlled by (a.b). This is one of the fastest adder so far. This circuit is simple but the power dissipation in this circuit is more than the 28T adder. But with same power consumption it performs faster [19][28].

C.14T FULL ADDER:

The 14T full adder has a 4 transistor PTL XOR gate, shown in Fig. 31, an inverter and two transmission gates for generating sum and C_{out} signals[19][31].

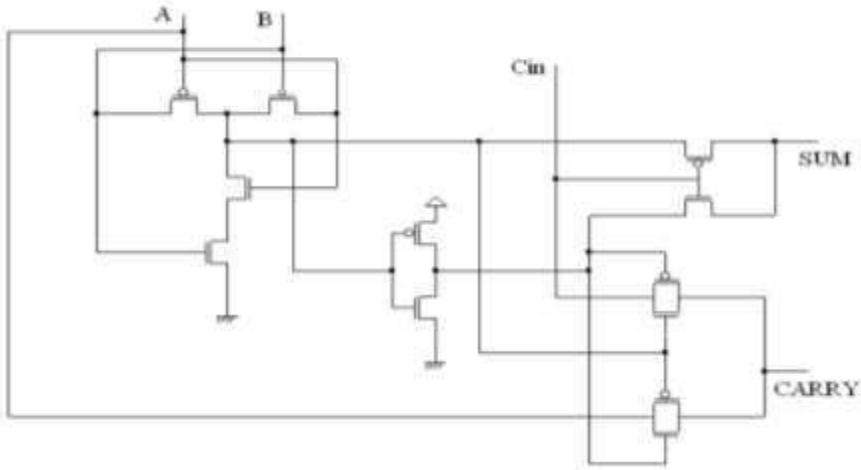

Fig. 3- T Full Adder[19][31]

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This circuit has a four transistor XOR which is inverted to generate XNOR. These XOR and XNOR are used to obtain SUM and C_{out}. TheC_{out} is generated by multiplexing A and C_{in} controlled by (a.b). This is one of the fastest adder and simpler than the conventional adder. In comparision with 28T adder the power dissipation in this circuit is higher. However with same power consumption it performs faster [24].

D.10T STATIC ENERGY RECOVERY FULL ADDER:

The energy recovering logic reuses charge and power consumption is less than non-energy recovering logic.

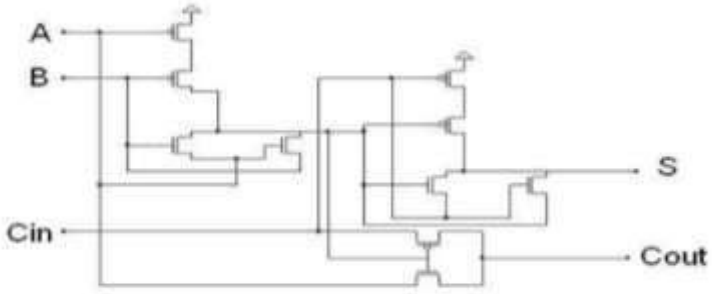

Fig. 4-T SERF Full Adder[19][32].

The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. The cout can be calculated by multiplexing A and C_{in} controlled by (A XOR B).Let us consider that there is a capacitor at the output node of the first XNOR module. To illustrate static energy recovery let us consider an example where initially A=B=0and then a changes to 1. When a and b both equals to zero the capacitor is charged by VDD. In the next stage when breaches a high voltage level keeping a fixed at a low voltage level, the capacitor discharges through a. Some charge is retained in a. Hence when a reaches a high voltage level we do not have to charge it fully. So the energy consumption is low here. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. The circuit produces full-swing at the output nodes. But it fails to provide so for the internal nodes. As the power consumption by the circuit reduces the circuit becomes slower. Also it cannot be cascaded at low power supply due to multiple threshold problems[19][32].

E. 10T FULL ADDERS REALIZED BY GATE DIFFUSION INPUT (GDI) STRUCTURES:

Now using these GDI based XOR and XNOR gates two different GDI based full adder architecture were designed [Fig. 19].

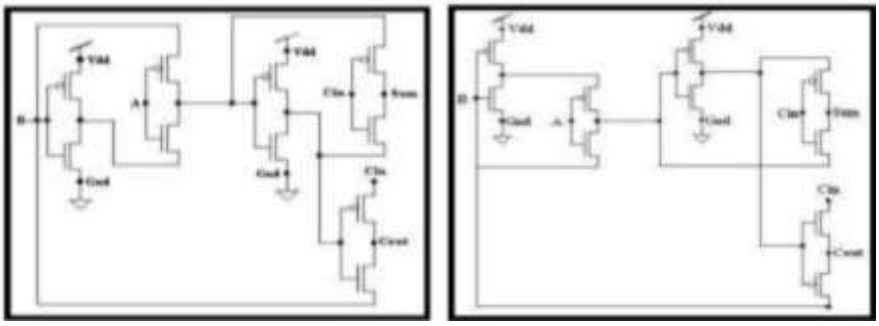

Fig. 5.(a)GDI XOR Adder[19][26] ***Fig. 5.(b) GDI XNOR Adder [19][26].***

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The circuit operation of GDI Based Full Adders is exactly the same as that of previous SERF module. Sum bit is obtained from the output of the second stage of XOR [Fig. 33(a)], XNOR[Fig. 33(b)] circuit while Carry bit (Cout) is calculated by multiplexing B and Cin controlled by (A XNOR B). These features give the GDI cell two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without huge amount of transistor count. The major problem of a GDI cell is that it requires twin-well CMOS or silicon on insulator (SOI) process to realize. Thus, it will be more expensive to realize a GDI chip. Moreover if only standard p-well CMOS process is used, the GDI scheme will face the problem of lacking driving capability which makes it more expensive and difficult to realize as a feasible chip[19][26].

F. ADDER 9A AND 9B:

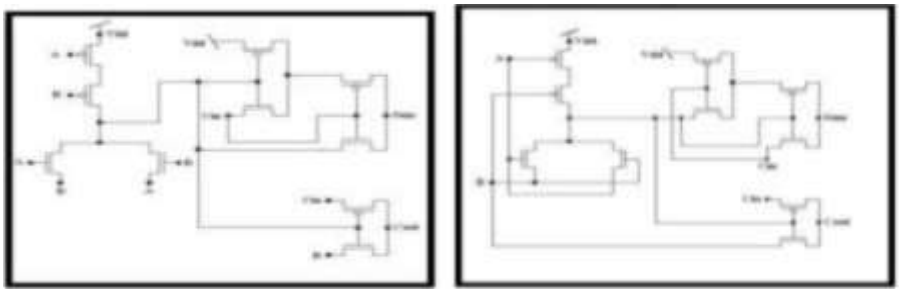

Fig. 6. (a) Adder 9A[19][33] *Fig.6. (b) Adder 9B[19][33].*

From the above figures (Fig 34a and 34b), we can see that a Static Energy Recovery XNOR gate is cascaded with the new G-XNOR gate to generate the Sum while the Cout function is implemented by simply multiplexing B and Cin controlled by (A XNOR B) as done in the previous circuits. These two new adders consistently consume less power in high frequencies and have higher speed compared with the previous 10-transistor full adders and the conventional 28-transistor CMOS adder [19][33].

G. 12T FULL ADDER:

An energy efficient single bit full adders with12 transistors using three transistor XOR gate [35], inverters and multiplexer blocks.

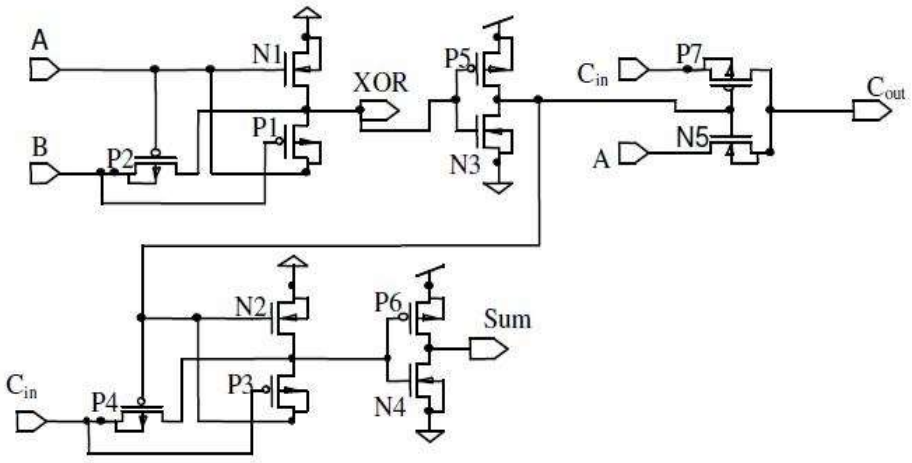

Fig.7. Full adder with 12- transistors[19][35]

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SIMULATION RESULTS

This section summarizes the simulation results. The simulations have been carried out on Symica Electronic Design Automation toolkit. This section comprises of wei et al 2011, 8-T adder cell, proposed 8-T full adder schematic designed in Symica Schematic Editor and rest of the figures are symica symprobe tool generated waveforms for various voltages and current. Although from the output waveforms, it is evident that power in an individual transistor is fluctuating, only average value of this power has been measured and calculated from the reading based on the output waveforms in symica symprobe tool.

Compared to the power consumption of 3.505 µW by wei et al 2011, 8-T adder cell, proposed 8-T full adder has a power consumption of only 0.404 µW.

The worst case delay of wei et al 2011, 8-T adder cell, proposed 8-T full adder full adder cell have been given in Table 5, calculated from the reading based on the output waveforms in symica symprobe tool, the worst case delay are measured to reach 90% of the steady state value. The total propagation delay is measured as:

$$\tau_P = \frac{\tau_{hl} + \tau_{lh}}{2} \quad \textbf{(3)}$$

CELL SCHEMATIC AND TRANSIENT RESPONSE OF PREVIOUS WORK

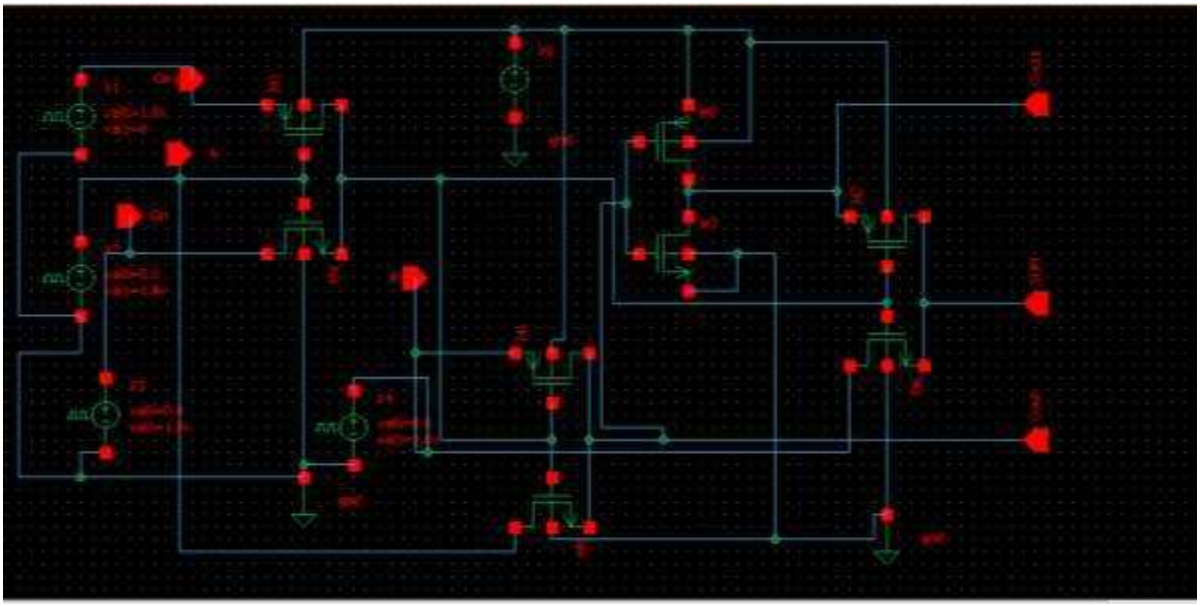

Fig. 8. Wei et al 2011 8-T full adder cell schematic in Symica DE software

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Fig. 9. Output waveforms of wei et. al. 2011 8-T adder in Symprobe software

CELL SCHEMATIC AND TRANSIENT RESPONSE OF PROPOSED WORK

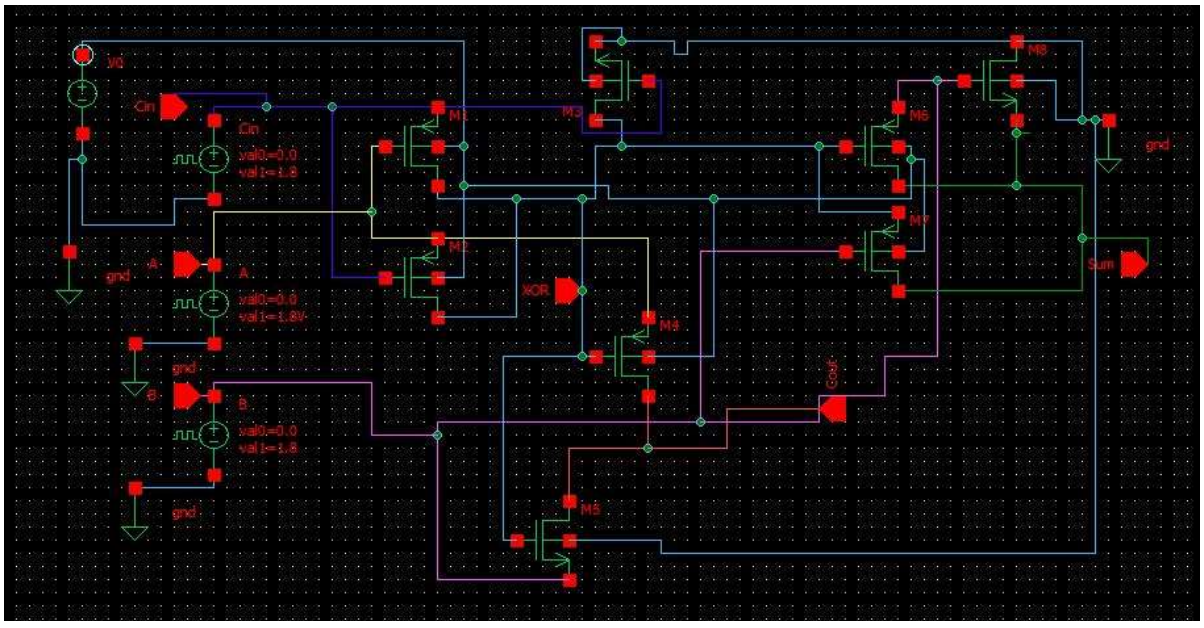

Fig. 10. Proposed 8-T CMOS full adder cell shematic

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Fig. 11. Simulation output waveforms in Symprobe software

EYE DIAGRAM OF PROPOSED 8-T FULL ADDER CELL

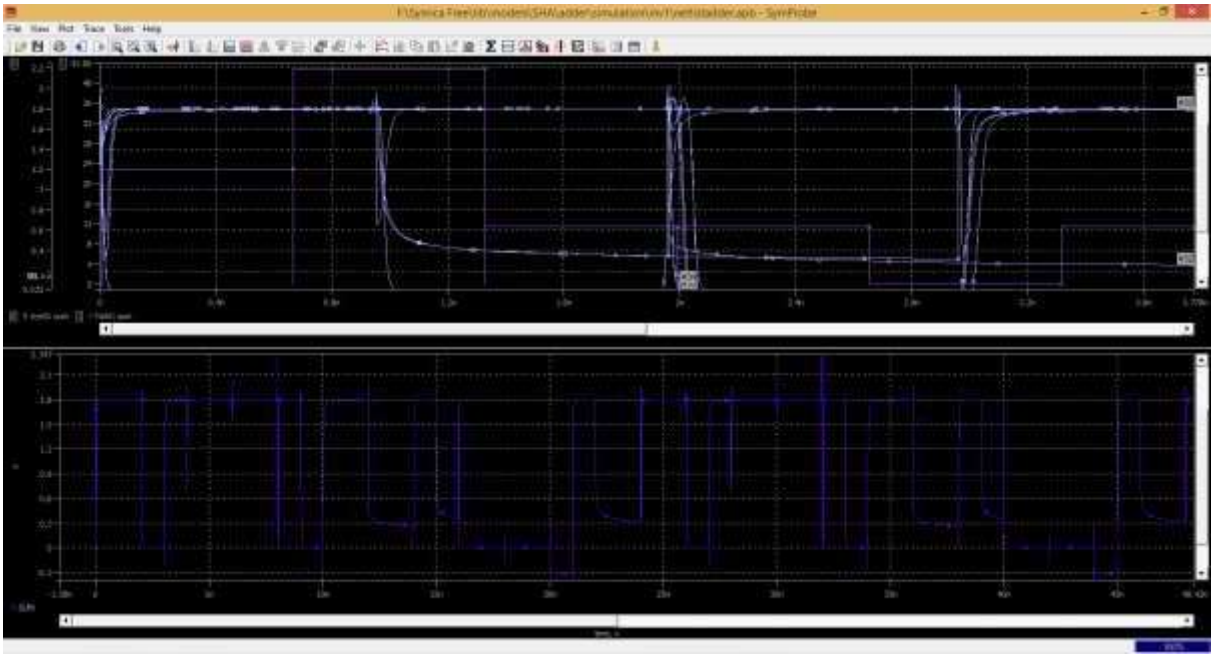

Fig. 12. Eye diagram of proposed 8-T adder in Symprobe software

The worst case delay for wei et al 2011, 8-T adder cell, proposed 8-T full adder cell have been given in Table 5. Compared to the propagation delay of 134.6 ps in wei et al 2011, 8-T adder cell, the proposed 8-T adder cell has a propagation delay of 119.5 ps.

CONCLUSION

This research work is an attempt to design a full adder Custom Cell Design using 8 transistors in 0.18 µm CMOS Technology. It involves use of 3-T XOR gate to implement the SUM circuit and Cout is implemented using a CMOS Multiplexer and suitable CMOS logic.

Total Power dissipation through wei et al 2011, 8-T adder cell and proposed 8-T full adder have been measured in the symica symprobe tool. A power dissipation of 3.505 µW and 0.404 µW have been obtained through wei et al 2011, 8-T adder cell, proposed 8-T full adder respectively. The best result has been obtained with the proposed adder cell. While comparing to the wei et al 2011, 8-T adder cell, proposed 8-T full addergives an advantage in terms of area, power, delay and power delay product.

This work analyzes the latest developments in low power circuit techniques and methods with an emphasis on speed improvement. Appropriate methods for transistor reduction are studied such as GDI(Gate Diffused Input), Pass transistor logic,etc[44][54]. The proposed work puts forth an8 transistor logic which is a modification over previous work proposed by wei et. al. 2011.

There is substantial reduction in transistor count as this full adder cell using only 8 transistors can be implemented as opposed to conventional 28-T standard CMOS technique.

Power dissipation of 0.404 µw and 3.505 µw have been obtained through Proposed 8-T adder cell and wei et al 2011, 8-T adder cell respectively. Proposed 8-T cell shows the best result in terms of power dissipation and area covered. The worst case propagation delay for proposed cell is 119.5x10-12 seconds and 134.6x10-12 seconds for wei et al 2011, 8-T adder cell.

The proposed work leaves a scope for future improvements related to sizing and area optimization of transistors used in Adder cell so that the power constraint could be taken care of and a smart layout can be prepare to optimize this result further.

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